In the Drawings:

Please replace original FIGS. 1 and 3 with replacement FIGS. 1 and 3.

Please add FIG. 4.

In the Specification:

Please amend the specification as indicated.

Page 5, kindly add the following paragraph after Paragraph 16:

FIG. 4 is a cross-sectional view of the n-channel embodiment of FIG. 1 having an n-type region laid out in a grid formation.

Page 7, Paragraph 20, kindly amend as follows:

An isolation trench 118 surrounds transistor 100 to isolate it from adjacent devices. FIG. 1 only shows the side portions of isolation trench 118; persons of ordinary skill in the art will recognize that portions of isolation trench 118 located in front of and behind the plane of the figure are not shown. A p-type implant may be made in trench ~~116~~ 118 as shown in FIG. 1.

Pages 7-8, Paragraph 21, kindly amend as follows:

In transistor 100, p-type region 106 is fully depleted by reverse biasing the n-type region with respect to both it and the p-type substrate 102. As an illustrative example, in

a device created with a 0.15 micron process, the sources and drains will have voltages of between about zero and 1.5 volts, n-type region 104 may be biased (Vn) at about 3.3 volts~~.~~, p-type region 106 may be charge-pump biased (Vp) at about -2 to about -3 volts, and substrate 102 may be biased (Vsub) at about -3 volts. The punch through of n-type layer 104 to the source region 108 and drain region 110 is greater than 3.3 volts but is fully depleted by the approximately -3 volts on the substrate 102. This serves to reduce the junction capacitance of the transistor 100 because the junction between N+ drain region ~~108~~ 110 and the fully depleted p-type region 106 has very little junction capacitance as compared with a standard transistor of the same generation without the fully depleted well. Persons of ordinary skill in the art will recognize that the bias voltages can readily be optimized for device-size scaling and different doping levels.

Page 8, Paragraph 22, kindly amend as follows:

In addition, because of the punch ~~trough~~ through of the n-type region 104 to the N+ source region 108 and drain region 110 and because p-type region 106 is fully depleted by the -3 volts on the buried p-type substrate layer 102, a field will sweep away any minority carriers to the n-type region 104, thus protecting the surface from being upset by a radiation pulse. Also, the transistor gamma is greatly reduced as change in charge of p-well 106 to the surface is small.

Page 8, Paragraph 24, kindly amend as follows:

According to one aspect of the invention, the n-type region 104 may be laid out in a grid formation, as shown in FIG. 4, to improve the impedance of minority carriers in depleted regions in order to avoid filling the wells with charge and thus changing the V_T of the device. FIG. 4 is merely one example of the n-channel embodiment of FIG. 1 having an n-type region laid out in a grid formation, with like elements numbered alike. The present invention is not intended to be limited to this one example. It is contemplated that other grid formations known in the art may be used as well.

Pages 11-12, Paragraph 31, kindly amend as follows:

In transistor 200, n-type region 204 is fully depleted by reverse biasing the n-type buried layers with respect to both it and the p-type substrate 202. As an illustrative example, in a 0.15 micron process, the sources and drains will have voltages of between about zero and 1.5 volts, n-type region 204 may be biased at about 3.3 volts which may be supplied by biasing the n-type buried regions 206 at about 3.3 volts, and substrate 202 may be biased at about -3 volts as a result of biasing the integrated for the n-channel devices. The punch through of p-type substrate layer 202 to the source region 208 and drain region 210 is greater than 3.3 volts but is fully depleted by the approximately +3 volts on the n+/n regions 206 and 204. This serves to reduce the junction capacitance of the transistor 200 because the junction between source region 208 and drain region 210 and the fully depleted n-type region ~~2046~~ 204 has very little junction capacitance. Persons